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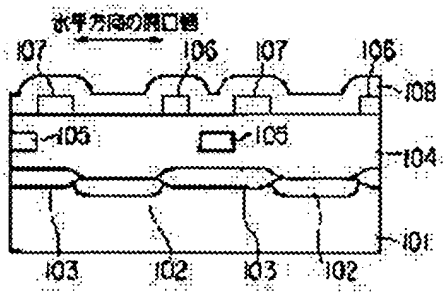
(54) MOS SOLID-STATE IMAGING DEVICE

(57)Abstract:

PROBLEM TO BE SOLVED: To form a device provided with a light-proof film structure which does not easily reflect the diagonal incident effective light beam when it is applied by forming a lower light-proof film.

SOLUTION: A silicon oxide film 104 is formed on a substrate 101, including a photodiode area 102 and a LOCOS layer 103 and an extending wiring 105 formed by polysilicon on the LOCOS layer 103 is imbecked in this silicon oxide film 104. A vertical signal line 106 and the power supply line 104 formed on the silicon oxide film 104 are formed as a first layer which is the lower layer of a plurality of metal layers by a metallic material having light-proof property such as aluminum. Therefore, since the light-proof film is formed by the first layer near the photodiode area 102, the incident light is will not shielded by this light-proof film and it is incident effectively to the photodiode area 102 for improving the level of photoelectric conversion signal.



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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the MOS mold solid state camera of a low noise especially with respect to an MOS mold solid state camera.
[0002]
[Description of the Prior Art] the well by which the conventional MOS mold solid state camera was formed on the p type semiconductor substrate -- the photodiode and the MOS transistor are formed in the layer. namely, a well -- a photodiode diffusion layer, the shutter gate, and an MOS transistor field are formed in the layer. the 1st metal layer for connecting the shutter gate and the gate of an MOS transistor -- a well -- it is insulated and formed on a layer. Moreover, it insulates on this 1st metal layer, and the 2nd metal layer is formed. This 2nd metal layer functions as an electric supply layer and a light-shielding film.
[0003]
[Problem(s) to be Solved by the Invention] Since the light-shielding film was formed with the 2nd layer metal according to the conventional MOS mold solid state camera, when slanting light carried out incidence, there was a problem that it was reflected by the light-shielding film and might not go into a photodiode. This invention makes the height of a light-shielding film low, and even when a slanting effective light enters, it aims at offering the solid state camera equipped with the light-shielding film structure which is hard to be reflected by the light-shielding film.
[0004]
[Means for Solving the Problem] The light-shielding film which prevents forming this invention on a semi-conductor substrate, and light carrying out incidence in addition to the photo-electric-conversion are recording section and this photo-electric-conversion are recording section, The magnification transistor which inputs the output of the photo-electric-conversion are recording section into a control electrode, and the perpendicular selection transistor which chooses Rhine which reads a signal, The image pick-up field which comes to arrange in procession two or more unit cells from which each is constituted by the reset transistor which resets the potential of the photo-electric-conversion are recording section, The power-source line connected to the magnification TORANJISU evening and a reset transistor, and two or more perpendicular signal lines arranged in the direction of a train in order to read the current of a magnification transistor, Two or more level selection transistors prepared in the end of a perpendicular signal line, and a level selection means to give a sequential selection pulse signal to the gate of a level selection transistor, In the solid state camera equipped with the level signal line which reads the signal current from a perpendicular signal line through a level selection transistor The solid state camera characterized by the metal layer which is the lowest layer of two or more metal layers, and forms either [at least] a power-source line or a perpendicular signal line having achieved the function of a light-shielding film is offered.
[0005] In the above-mentioned solid state camera, a power-source line is arranged in the same parallel direction as a perpendicular signal line, the both line is formed in the layer [1st] metal layer, and

horizontal aperture width of the photo-electric-conversion are recording section is characterized by what is prescribed by the power-source line and the perpendicular signal line.
[0006] In the above-mentioned solid state camera, it is characterized by for two wiring layers, a layer [1st] metal layer and a layer [2nd] metal layer, having achieved the function as a light-shielding film, and for the horizontal aperture width of the photo-electric-conversion are recording section being prescribed by a power-source line and the perpendicular signal line, and specifying vertical aperture width in the layer [2nd] metal layer.
[0007] The magnification transistor which this invention is formed on a semi-conductor substrate, and inputs the output of the photo-electric-conversion are recording section and the photo-electric-conversion are recording section into a control electrode, Connector wiring for inputting the signal output from the photo-electric-conversion are recording section into a magnification transistor, The image pick-up field which comes to arrange in procession two or more unit cells from which each is constituted by the perpendicular selection transistor which chooses Rhine which reads a signal, and the reset transistor which resets the potential of the photo-electric-conversion are recording section, The power-source line of a magnification transistor and a reset transistor, and two or more perpendicular signal lines arranged in the direction of a train in order to read magnification tolan Sister's current, Two or more level selection transistors prepared in the end of a perpendicular signal line, and a level selection means to give a sequential selection pulse signal to the gate of a level selection transistor, In the solid state camera equipped with the level signal line which reads the signal current from a perpendicular signal line through a level selection transistor, the solid state camera characterized by forming the wiring layer which forms connector wiring by the wiring layer near [wiring layer / which forms a perpendicular signal line] a substrate is offered.
[0008]
[Embodiment of the Invention] Hereafter, the operation gestalt of this invention is explained with reference to a drawing. The circuit of the MOS mold solid state camera concerning the 1st operation gestalt of this invention is shown in drawing 1 , and the configuration of the unit cell of the solid state camera of drawing 1 is shown in drawing 2 .
[0009] According to the solid state camera of drawing 1 , two or more unit cells 11 are arranged in the matrix direction, and these unit cells 11 are read in the perpendicular selection line 12 and reset line 13 list, and are connected to the perpendicular shift register 15 through a line 14. Moreover, these unit cells 11 are connected to the level signal line 18 through the perpendicular signal line 16 and the level selection transistor 17. The gate of the level selection transistor 16 is connected to the level shift register 19, and the level selection transistor 17 is alternatively turned on by the signal from the level shift register 19. Thereby, the signal of the perpendicular signal line 16 is read into the level signal line 18. Furthermore, the power-source line 20 and the load transistor 21 are connected to a unit cell 11.
[0010] Drawing 2 shows the structure of the 2 pixels [per unit] unit cell 11, i.e., the unit cell of 2 pixel/unit. According to this, two photodiodes 31a and 31b are formed in the cel 11, and these photodiodes 31a and 31b are connected to the power-source line 20 through the reset transistor 35 while connecting with the gate of the magnification transistor 33 through the read-out transistors (shutter gate transistor) 32a and 32b.
[0011] The perpendicular signal line 16 is connected to the power-source line 20 through the magnification transistor 33 and the perpendicular selection transistor 34 at a serial. The selection line (address line) 12 is connected to the gate of the perpendicular selection transistor 34.
[0012] In the unit cell 11 of the above-mentioned configuration, if it reads on the reading line 14 and a signal enters, the read-out transistors 32a and 32b will serve as ON, the photo-electric-conversion signal of Photodiodes 31a and 31b will read, and it will be inputted into the magnification transistor 33 through Transistors 32a and 32b. If a selection signal is supplied to the selection line 12 at this time, the perpendicular selection transistor 34 will serve as ON, and the photo-electric-conversion signal amplified by the magnification transistor 33 will be read to the perpendicular signal line 16.
[0013] If a reset signal goes into the reset line 13, the reset transistor 35 will serve as ON and a unit cell 11 will be reset. Drawing 3 shows the flat-surface pattern of the unit cell 11 shown in drawing 2 , and

drawing 4 shows the cross section of the unit cell which met the A-A line of drawing 3 .
[0014] As shown in drawing 4 , they are the photo-electric-conversion are recording field 102, i.e., a photodiode field, and LOCOS to a substrate 101. The layer 103 is formed by turns. The photodiode field 102 and LOCOS The laminating of the silicon oxide 104 is carried out on a substrate 101 including a layer 103. In this silicon oxide 104, it is LOCOS. The bond wiring 105 formed by polish recon on a layer 103 is laid underground.
[0015] The perpendicular signal line 106 and the power-source line 107 are formed in silicon oxide 104 top face. The laminating of the passivation membrane 108 is carried out on the silicon oxide 104 containing the perpendicular signal line 106 and the power-source line 107.
[0016] In the structure of the above unit cells, the perpendicular signal line 106 and the power-source line 107 which were formed on silicon oxide 104 are formed as the 1st layer which is the lowest layer of two or more metal layers. Although the upper layer of the 2nd more than layer is not shown in drawing 4 , since a circumference circuit, for example, a perpendicular shift register, a level shift register, etc. are constituted, it is formed.
[0017] It is formed of said metal which has protection-from-light nature, such as aluminum, and gets down, and 106 and 107 [layer / 1st] function also as a light-shielding film to incident light. Conventionally, since this light-shielding film is formed with the metal of the 2nd layer separated from the photodiode as shown in drawing 5 B, the incident light which the macro lens converged is reflected by this light-shielding film of the 2nd layer, and its light which carries out incidence to a photodiode decreases. It will be reflected by this light-shielding film and incidence especially of most light which carries out incidence from across will not be carried out to a photodiode.
[0018] On the other hand, in this invention, since the light-shielding film is formed of the 1st layer near the photodiode field 102, without being shaded by this light-shielding film, incidence of the incident light is efficiently carried out to the photodiode field 102, and it raises the level of a photo-electric-conversion signal.
[0019] Drawing 6 and drawing 7 show the cross section of the solid state camera of the 2nd operation gestalt, drawing 6 is a horizontal cross section, i.e., the cross section which met the A-A line of drawing 3 , and drawing 7 is a vertical cross section, i.e., the cross section in alignment with B-B of drawing 3 .
[0020] According to this operation gestalt, as shown in drawing 6 , they are the photodiode field 102 and LOCOS like [a substrate 101] the 1st operation gestalt. A layer 103 is formed and the bond wiring 105 is laid under the silicon oxide 104. The perpendicular signal line 106 and the power-source line 107 are formed as the 1st layer on silicon oxide 104, and silicon oxide 109 is further formed on it. This 1st layer (106,107) functions as a light-shielding film to the 1st direction. Furthermore, the metal layer 110 prolonged in the 2nd direction which intersects perpendicularly in the 1st direction, for example, an aluminum layer, is formed on silicon oxide 109. This aluminum layer 110 shades the 2nd direction to protection from light of the 1st direction by the 1st layer (106,107). A passivation membrane 108 is formed in silicon oxide 109 top face including this aluminum light-shielding film 110.
[0021] Moreover, as shown by the vertical section of drawing 7 , the gate polish recon layer 111 is formed on the silicon substrate 101. These polish recon layer 111 is used as a mask, when forming the photo-electric-conversion are recording field 102, i.e., a photodiode field, by the self aryne (self align). That is, this gate polish recon layer 111 has prescribed the die length of the photodiode field 102.
[0022] Also in this operation gestalt, since the 1st layer which constitutes the perpendicular signal line 106 and the power-source line 107 functions as a light-shielding film, the effectiveness of this invention which was explained by drawing 5 can be attained.
[0023] Drawing 8 shows the cross section along the perpendicular direction of the solid state camera of the 3rd operation gestalt. According to this operation gestalt, they are the photodiode field 102 and LOCOS like [a substrate 102] the above-mentioned operation gestalt. A layer 103 is formed. On it, the gate polish recon layer 111 is formed. This gate polish recon layer 111 can be used as a mask for forming the photo-electric-conversion are recording field 103, i.e., a photodiode field, by the self aryne like the operation gestalt of drawing 7 .
[0024] The laminating of the silicon oxide 104 and 109 is carried out to a silicon substrate 101 one by

one like the above-mentioned operation gestalt. On bottom silicon oxide 104, although not illustrated, the perpendicular signal line 106 and the power-source line 107 as the 1st layer are formed, and the layer [2nd] metal layer 110 is formed on top silicon oxide 108. That is, the layer [1st] metal layer 106, i.e., a perpendicular signal line, and the power-source line 107 function as a light-shielding film to the 1st direction, and the layer [2nd] metal layer 110 functions as a light-shielding film to the 1st direction and the 2nd crossing direction.

[0025] A passivation membrane is formed on top silicon oxide 108 including the 2nd light-shielding film 110. The 1st layer functions as the same light-shielding film as the above-mentioned 1st and 2nd operation gestalt, incident light is not shaded un-wanting, improvement in the sensibility of a unit cell can be aimed at, and this 3rd operation gestalt can also shade the direction where the 1st layer moreover intersects perpendicularly by the 2nd layer.

[0026] In addition, although the perpendicular signal line 106 and the power-source line 107 are formed in the layer [1st] metal layer, [in / both / each above-mentioned operation gestalt] It is good also as a layer which is different in both by forming a perpendicular signal line in the layer [1st] metal layer which functions as a light-shielding film which determines horizontal opening, for example, and forming a power-source line in the layer [2nd] metal layer which functions as a light-shielding film which determines vertical opening, without restricting to this.

[0027] Drawing 9 shows the cross section of the solid state camera of the 4th operation gestalt. This operation gestalt has the configuration which makes as small as possible capacity of the gate of the magnification mold transistor included in the detecting element of an MOS mold solid state camera, i.e., a unit cell, and raises sensibility. That is, since the sensibility of a unit cell is in inverse proportion to the capacity of a detecting element, it is desirable to make capacity of a detecting element as small as possible. Then, a detecting element is constituted so that the wiring layer of a detecting element, especially a magnification mold transistor may be separated as much as possible from other wiring layers.

[0028] That is, according to the unit cell of drawing 9 , n mold impurity range 112 used as the source of an MOS transistor (namely, MOS transistors 32a or 32b of drawing 2) which functions on a silicon substrate 101 as the photo-electric-conversion are recording field 102, i.e., a photodiode field, and the shutter gate, or a drain field is formed. The gate polish recon 113 is insulated and formed on the silicon substrate 101 among fields 102 and 112. This gate polish recon serves as a gate electrode of a shutter gate transistor.

[0029] In the right-hand side of this drawing, it insulates on a silicon substrate 101, and the gate polish recon layer 114 is formed. This gate polish recon layer 114 serves as a gate electrode of the magnification transistor 33 shown in drawing 2 . The polish recon layer 115 for bond wiring which connects this gate polish recon layer 114 and n mold impurity diffused layer 112 is formed in the bottom silicon oxide 104 side.

[0030] The perpendicular signal line 106 which consists of an aluminum layer is formed on bottom silicon oxide 104. This perpendicular signal line 106 serves as a layer [1st] metal layer which functions as a light-shielding film. The laminating of the top silicon oxide 109 is carried out on silicon oxide 104 including this 1st layer 106.

[0031] The aluminum layer 110 as 2nd metal layer is formed on the above-mentioned top silicon oxide 109. The 2nd layer, 110 is formed in this direction that intersects the 1st layer, and functions as a light-shielding film to this crossover direction. A passivation membrane 108 is formed on top silicon oxide 109 including this 2nd layer 110.

[0032] the wiring layer of others [wiring layer / 115 / which is connected with n mold impurity diffused layer 112 from which the gate polish recon layer 114 which constitutes the gate of a magnification mold transistor, and this polish recon layer 114 constitute a shutter transistor according to the above-mentioned configuration / bond], for example, the 1st, -- layer 106 -- and it brings close to a silicon substrate 101, and is formed as the 2nd layer can be separated from 110. Therefore, the parasitic capacitance formed between the gate polish recon layer 114 and the bond wiring layer 115, the 1st layer, and the 2nd layer becomes small, and the sensibility of the detecting element of a unit cell improves.

[0033]
[Effect of the Invention] Since the metal layer of the 1st layer, i.e., the lowest layer, is used as a protection-from-light layer in the solid state camera wired using two or more metal layers according to this invention, it is not reflected in un-wanting by the protection-from-light layer, namely, an eclipse does not produce incident light, incidence of the incident light is efficiently carried out to a photo-electric-conversion are recording field, i.e., a photo transistor field, and it raises the sensibility of a solid state camera.
[0034] Moreover, it is formed so that it may shade in the direction in which the layer [2nd] metal layer which is the upper layer of the light-shielding film formed by the 1st layer intersects the light-shielding film of the 1st layer. That is, protection from light is possible about two directions which cross by the light-shielding film of the 1st layer and the 2nd layer. Therefore, the incidence only of the effective light which eliminated light [**** / the scattered light etc. / un-] can be carried out to a photo-electric-conversion are recording field.
[0035] Moreover, since it is used as a mask for the gate polish recon layer formed on a silicon substrate to form a photo-electric-conversion are recording field by the self aryne, the die length of a photo-electric-conversion are recording field can set up correctly.
[0036] Moreover, since it is constituted so that an MOS mold solid state camera may separate the wiring layer of the detecting element, especially a magnification mold transistor from other wiring layers as much as possible, capacity of the gate of a magnification mold transistor is made as small as possible, and the sensibility of a detecting element improves.

[Translation done.]

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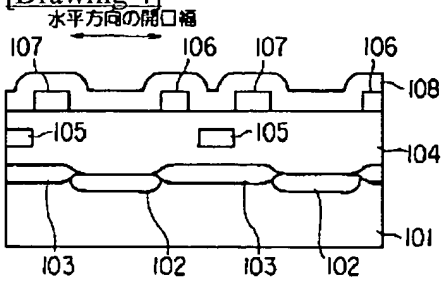
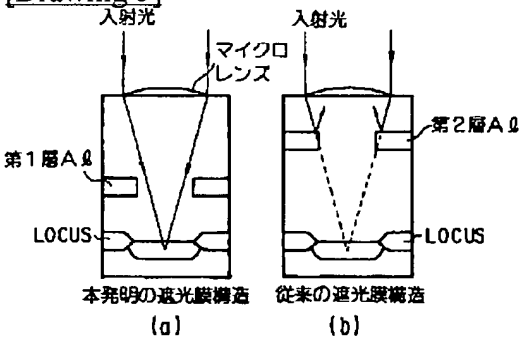
DRAWINGS

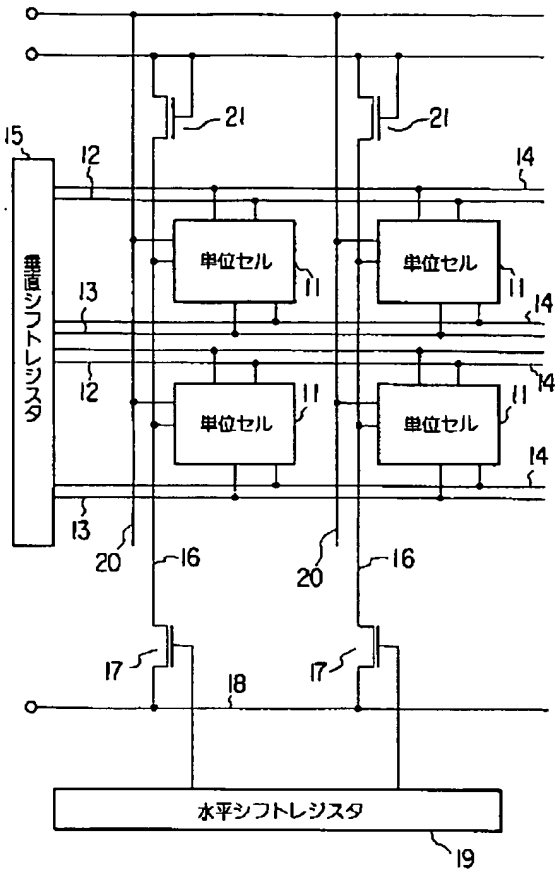
[Drawing 4]



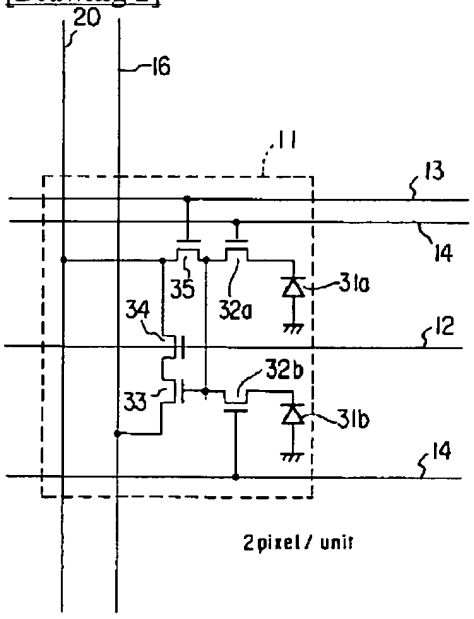
[Drawing 5]



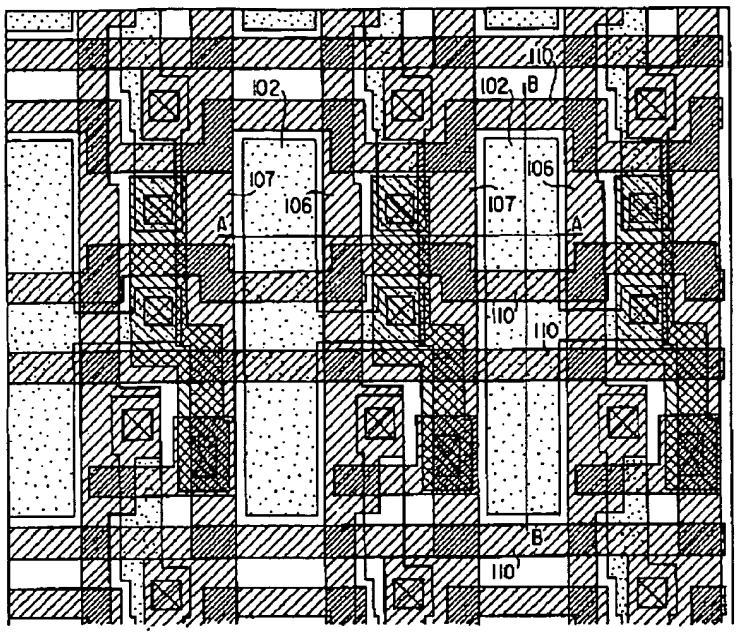
[Drawing 1]



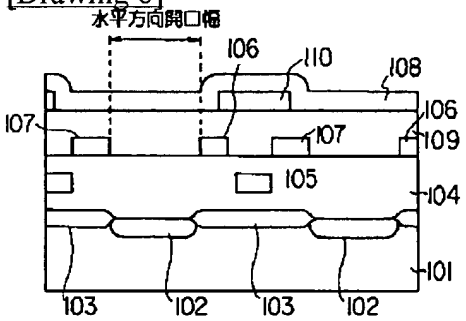
[Drawing 2]



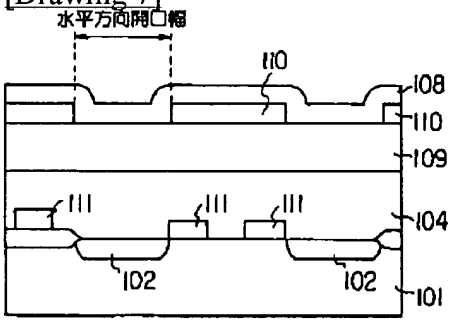
[Drawing 3]



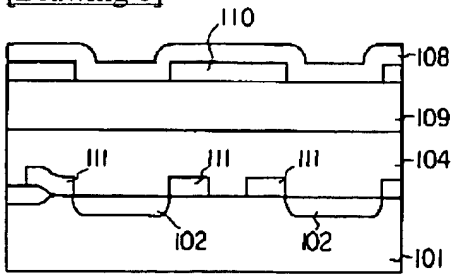
[Drawing 6]



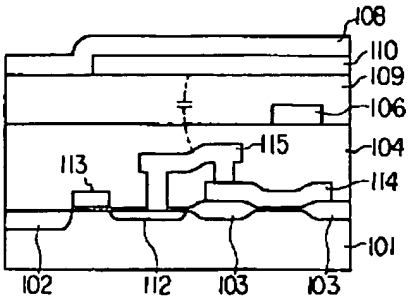
[Drawing 7]



[Drawing 8]



[Drawing 9]



[Translation done.]